



# UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE  
United States Patent and Trademark Office  
Address: COMMISSIONER FOR PATENTS  
P.O. Box 1450  
Alexandria, Virginia 22313-1450  
www.uspto.gov

SN

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/777,677	02/13/2004	Nicholas J. Stone	Q79884	5876
23373	7590	02/09/2005	EXAMINER	
SUGHRUE MION, PLLC 2100 PENNSYLVANIA AVENUE, N.W. SUITE 800 WASHINGTON, DC 20037			HA, NGUYEN T	
			ART UNIT	PAPER NUMBER
			2831	

DATE MAILED: 02/09/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

## Office Action Summary

Application No.

10/777,677

Applicant(s)

STONE ET AL.

Examiner

Nguyen T Ha

Art Unit

2831

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

### Status

- 1) ☒ Responsive to communication(s) filed on 17 November 2004.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

### Disposition of Claims

- 4) ☒ Claim(s) 1-17 is/are pending in the application.
- 4a) Of the above claim(s) 3,4 and 8-17 is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1,2 and 5-7 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

### Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

### Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☒ None of:
- 1) ☒ Certified copies of the priority documents have been received.
  - 2) ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  - 3) ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

### Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)  
Paper No(s)/Mail Date 0904.
- 4) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date. \_\_\_\_\_.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: \_\_\_\_\_.

## **DETAILED ACTION**

### ***Election/Restrictions***

1. Applicant's election with traverse of embodiment I (claims 1-2 and 5-7) in the reply filed on 11/17/2004 is acknowledged. The traversal is on the ground(s) that embodiment II, III and IV would be co-extensive. This is not found persuasive because the other embodiments would be classified in a different class than claims 1-2 and 5-7.

The requirement is still deemed proper and is therefore made FINAL.

### ***Claim Objections***

2. Claims 6-7 are objected to because of the following informalities:

Claims 6-7, line 1, "the semiconducting layer" lacks antecedent basis.

Appropriate correction is required.

### ***Claim Rejections - 35 USC § 102***

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1-2 are rejected under 35 U.S.C. 102(b) as being anticipated by Barber et al. (US 6,242,989).

Regarding claim 1, Barber et al. disclose a use as a non-linear capacitor of an electronic device (figures 3-6) including first (516), second (522) and third conductor layers (508) respectively arranged as the source, drain and gate electrodes of a field effect transistor (T1 figure 20), the third conductor layer (508) being capacitively coupled

with both the first and second conductor layers (figure 5), wherein the use includes applying an alternating voltage (V1) across the third conductor layer and either of the first and second conductor layers whilst leaving the other of the first and second conductor layer at a floating potential (figure 5).

Regarding claim 2, Barber et al. disclose the third conductor layer (508) is capacitively coupled with the second conductor layer to a greater degree than with the first conductor layer, and wherein an alternating voltage (V1) being applied across the first (516) and third conductor layers (508) whilst leaving the second conductor layer at a floating potential (figure 6).

***Claim Rejections - 35 USC § 103***

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

6. Claims 5-7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Barber et al. (US 6,242,989) in view of Dimitrakopoulos et al (US 6,344,662).

Regarding claim 5, Barber et al. disclose all the claimed limitations discussed above with respect to claim 1, except for the layers constituting the field effect transistor is deposited by solution processing (column 5, lines 54-62).

Dimitrakopoulos et al. teach the layers constituting the field effect transistor is deposited by solution processing (column 5, lines 54-62).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to use the process of Dimitrakopoulos et al. in Barber et al., in order to improve the quality and enhance the dielectric constant.

Regarding claim 6, the teaching of Dimitrakopoulos et al. includes the semi-conducting layer of the field effect transistor is a molecular organic semiconductor (column 5, lines 23-28).

Regarding claim 7, the teaching of Dimitrakopoulos et al. includes the semi-conducting layer of the field effect transistor is a conjugated polymer semiconductor (column 5, lines 23-28).

#### **Citation Relevant of Prior Art**

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

a. Alping et al. (US 6,380,600) disclose micro-electromechanical arrangement.

b. Cao (US 6,674,116) discloses variable capacitor using MOS gated diode with multiple segments to limit DC current.


**Conclusion**

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nguyen T. Ha whose telephone number is 571-272-1974. The examiner can normally be reached on Monday-Friday from 8:30AM to 6:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Dean Reichard can be reached on 571-272-2800 ext. 31. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

**Nguyen T. Ha**  
**February 3, 2005**

  
DEAN A. REICHARD  
SUPERVISORY PATENT EXAMINER  
TECHNOLOGY CENTER 2800